REMARKS

The objections, rejections and comments of the Examiner set forth in the Office Action dated December 10, 2003 have been carefully reviewed by the Applicant. Claims 33-42 have been canceled. Claims 1-32 remain pending.

Rejections under 35 U.S.C. 112, first paragraph

Claims 1, 10, 20 and 26 are currently rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirements. It is purported that the claims include subject matter not described in the specification in such as way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time of the filing of the application, had possession of the claimed invention.

Applicant respectfully traverses the above rejections. As disclosed in paragraph 5 of the present specification, a time stamp "has two components. The first component is the specific clock cycle of the reference clock within which the event occurs. The second component is the time at which the event occurs within the specific clock cycle of the reference clock." Thus, the specification of the present invention satisfies the written description requirement with respect to a system and method for "timestamping events with a resolution of less than one clock cycle in a signal."

Rejections under 35 U.S.C. 103(a)

Claims 1 and 10 are currently rejected under 35 U.S.C. 103(a) as being anticipated by Chen et al. (US 5,642,478) in view of Baum et al. (USP 5,815,634). Claims 1-5 and 10-14 are currently rejected under 35 U.S.C. 103(a) as being

anticipated by Adelmann et al. (US 4,894,823) in view of Baum et al. Claims are currently rejected under 35 U.S.C. 103(a) as being anticipated by Boereker et al. (US 2003/0035502A1) in view of Baum et al. Applicant respectfully traverses these rejections.

The argument presented herein below are directed to Claims 1 and 10, but are equally applicable to Claims 1-5 and 10-14 rejected under Adelmann in view of Baum and Claims 20-25 rejected under Boereker et al. in view of Baum.

In response, Claims 1 and 10 have been amended to more clearly distinguish the present claimed invention from Chen. It is suggested that the combination of Chen and Baum teach or suggest "timestamping an event with a resolution of less than one clock cycle."

However, Chen does not teach or suggest a timestamp or the act of timestamping events with a resolution of less than one clock cycle. Chen teaches a timestamp for a block of data, and the timestamp is derived from an internal clock 58. One with normal skill in the art would recognize that a typical system internal clock depends upon counting an integral number of clock cycles, and thus would have a resolution that is not less than a clock cycle.

Furthermore, Baum discloses an apparatus for controlling playback of audio and video signals from an encoded stream comprising at least audio data packets, video packets, audio presentation time stamps and video presentation time stamps. Baum further discloses a synchronization resolution of one half frame, with "an allowable time drift of approximately one half of 33.33 milliseconds or 16.67 milliseconds," where "a resolution of one half frame synchronization may require a time drift of less than 1500 SCLK clock cycles." (Col. 8, lines 4-11) Thus Baum fails to disclose any teachings for an apparatus or method for timestamping with a

resolution of less than one clock cycle. The best resolution Baum discloses is in the order of half a frame equivalent to 1500 clock cycles.

Thus, no combination of Chen and Baum teaches or suggests a method and apparatus of "timestamping with a resolution of one clock cycle," as claimed by the present invention.

Lastly, Baum's patent relates to multimedia systems and time stamping of audio and video files, for synchronization and decoding /decompressing video images and audio files. Chen relates to debugging facility fro tracing hardware and software faults in distribute d digital systems. Simply nowhere does Chen or Baum include any teachings or suggestion to combine the two references.

Adelmann is directed to the handling of data as packets or streams, and are not concerned with the timing of events with a resolution of less than a clock cycle. Boerker is directed to a data reception circuit . One with normal skill in the art would recognize that the clocks relied upon by Adelmann and Boerker would not have a resolution of less than one clock cycle, as claimed in the present invention.

Conclusion

In summary, in light of the arguments presented herein, Applicant asserts that Claims 1-32 are now in condition for allowance and earnestly solicit such action by the Examiner.

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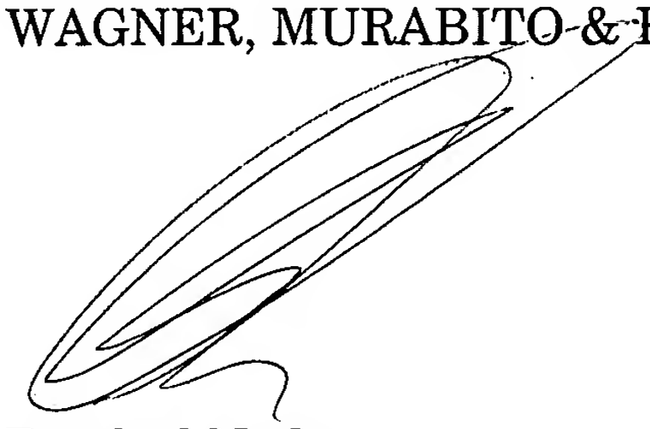
Respectfully submitted,

WAGNER, MURABITO & HAO LLP



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